Testing High-Speed Protocol Based Rambus™ DRAMs

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Abstract

Testing new high-speed protocol based memories such as Direct RDRAM™ offers new opportunities for memory manufacturers and test engineers to re-optimize their test strategies. Identifying the critical circuit parameters, and selecting the proper equipment and test fixtures for their measurement, is crucial to achieving maximum throughput, yield and performance of the finished products. This paper outlines key test techniques required by the high-density structure and high bandwidth operation of RDRAM™ devices, and suggests approaches to their application in a production test environment.

Introduction

The continuous quest for improvements in integrated circuit design and semiconductor manufacturing techniques have made possible microprocessors with higher and higher clock speeds, which places increasing demands on the I/O interface to memory devices and other peripherals. To meet these demands, DRAM manufacturers are deploying new chip designs and memory architectures that significantly increase both density and I/O bandwidth.

The Direct RDRAM developed by Rambus Inc. redefines the memory subsystem by melding a high density DRAM with a very high bandwidth interface. To achieve data transfer rates beyond 800 Mbits/sec, Direct RDRAM employs special interface and addressing techniques to mask the internal clock delay of traditional DRAMs.

Due to the high-speed interface and protocol associated with Rambus RDRAM, there are three major concerns that test engineers must address to ensure full, at-speed production testing of a Rambus device:

1. Existing highly parallel memory test systems (32-64 devices in parallel) cannot provide the 800+ MHz data rates required to test Direct RDRAM devices.

2. Even at lower speeds, the RDRAM access protocol and interleaving scheme are not supported by today's mainstream memory test systems.

3. Only the highest performance testers available on the market today can make the critical timing measurements for Direct RDRAM devices. These testers offer set-up and hold time measurements of < 200 ps, but few of them can deliver it to the DUT. The accuracy required for testing Direct RDRAM devices (150-200 ps) also means that traditional guardband methods may result in unacceptably high yield losses.

One method to address these issues with test systems available today makes use of a two-pass final test strategy. For one of the passes, DRAM manufacturers can use existing low speed memory testers for long- and short- cycle testing. Long cycle testing deals primarily with core data retention by stressing the $t_{ras\text{-}max}$ (maximum word-line high time) and $t_{ref\text{-}max}$ (maximum refresh interval) specifications of the device. Long-cycle tests can also be used to create noise patterns on critical write and read cells in rows adjacent to the target row. Since long-cycle tests are performed on each row of the core array, they represent the highest percentage of test time at wafer sort and final test. Short-cycle testing exercises the high-speed data access operation of the part. These test patterns invoke worst case access times by stimulating directional changes on busses, decoder critical paths, etc.

Both test types can be performed either in normal mode on high-speed memory testers or in a special test mode supported by the Direct RDRAM architecture called DAMode (direct access mode). DAMode bypasses the access protocol to allow the test engineer to test the core at standard DRAM core speeds so that a lower speed (<100 MHz) memory test system can be used. DAMode details are not covered in this paper but are available to Rambus licensees directly from Rambus Inc. DAMode allows conventional memory test systems to test the Direct RDRAM core with standard DRAM test flows and patterns.

Considering that long-cycle tests account for 90% of the overall test time at final test, DAMode can play a significant role in reducing the number of new high-end testers needed for a given production run-rate.

The remainder of the two-pass strategy deals with the functional tests of the interface logic and AC timing measurements. This requires high-speed logic test capability to speed sort and test the critical high speed timing measurements of the RDRAM interface to verify the interface logic as well as the tight timing tolerances of the RDRAM devices. Fortunately, interface test time is much

shorter than the time needed to test the core, so fewer high-end testers are required than conventional, lower speed test systems.

The two-pass strategy gives Direct RDRAM manufacturers the option to choose their own mix of high-end and lower speed test systems to optimize throughput requirements while keeping capital costs and cost of test down. For example, unnecessary second-pass testing can be avoided by first testing the section of the device with the lowest expected yield.

Table-1 shows how test floor resources might be allocated for the two-pass method:

Table-1: Two-Pass Test Strategy

Flow	Device Form	Tester Class	Mode	Typical Test Items
Wafer Sort	Wafer	Conventional Memory Tester	DAMode	Redundancy Analysis
Laser Repair	Wafer	NA	NA	NA
Final Wafer Sort	Wafer	Conventional Memory Tester	DAMode	Reject Fail Die
Assembly	Wafer/Package	NA	NA	NA
1st Package Test	Package	Conventional Memory Tester	DAMode	Opens/Leakage
Burn-In	Package	NA	DAMode	Hold
2nd Package Test	Package	Conventional Memory Tester	DAMode	Leak, Hold, Pattern Dependency
Final Package Test	Package	HP 95000 HSM Series	Normal Mode	Speed Grade

In the "single-pass" test strategy, post burn-in core tests and Rambus interface tests are combined during a single insertion on a high-speed test system.

Recently introduced test systems have the ability to test RDRAM devices with a single insertion, either by testing the core at the RDRAM interface speeds or by testing the core using DAMode. However, regardless of whether a two-pass or single-pass test strategy is used, demands of the high-speed tests must be met in order for the test engineer to maximize the yield of the RDRAM devices. Accurately driving and comparing > 800 Mbit/s address, control and data signals, without I/O bus contention problems, requires extremely high speed and accurate test equipment and electrical interfacing to the handler. Careful consideration must be given to the design of the loadboard, DUT (Device Under Test) board, and selecting the high-speed contactors to minimize inaccuracies added by these components.

In the following sections, we will review the Direct RDRAM operation in general and discuss the critical timing parameters and their effect on the issues just described. Clock and data rate requirements, I/O bus contention issues, accuracy, and loadboard and contactor design considerations will be discussed. Along with these critical testing issues, the solutions implemented in the HP 95000 High Speed Memory (HSM) Series test system will be explained.

Direct RDRAM Data Rates

The Direct RDRAM specification currently supports 300 MHz and 400 MHz clock devices with 600 Mbit/s and 800 Mbit/s data rates, respectively. The interface of the Direct RDRAM connects to the Rambus Channel, an 18-bit wide bi-directional data bus and 8-bit wide Address and Control bus that is optimized for block data transfer for a given clock speed. To read data from the Direct RDRAM, a processor uses the Rambus Channel to send a request packet to the RDRAM. The packet contains multiple bytes including the requested address and additional control information. In the case of the 800 Mbit/s device, dual bytes are valid on the channel only during the 1.25 ns period. After receiving the request packet, the Direct RDRAM verifies the presence of the requested data in its core, accesses the data, and sends it back to the controller at a 1.25 ns per dual-byte rate. A write transaction to the RDRAM is similar to read, except that the controller provides the data. A typical read/write packet sequence is shown in the following figures. Reads and writes have the same timing to avoid pipeline bubbles when mixed R/W sequences occur.

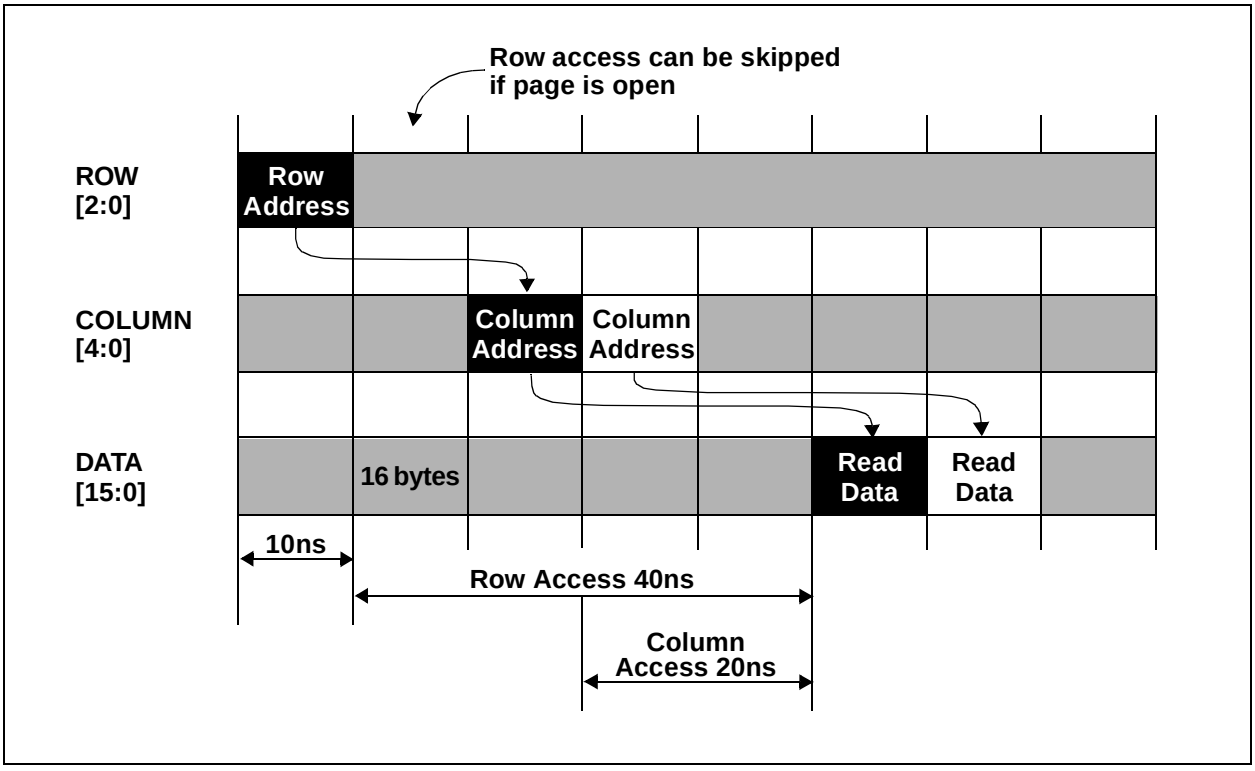

Figure-1 Read Transaction

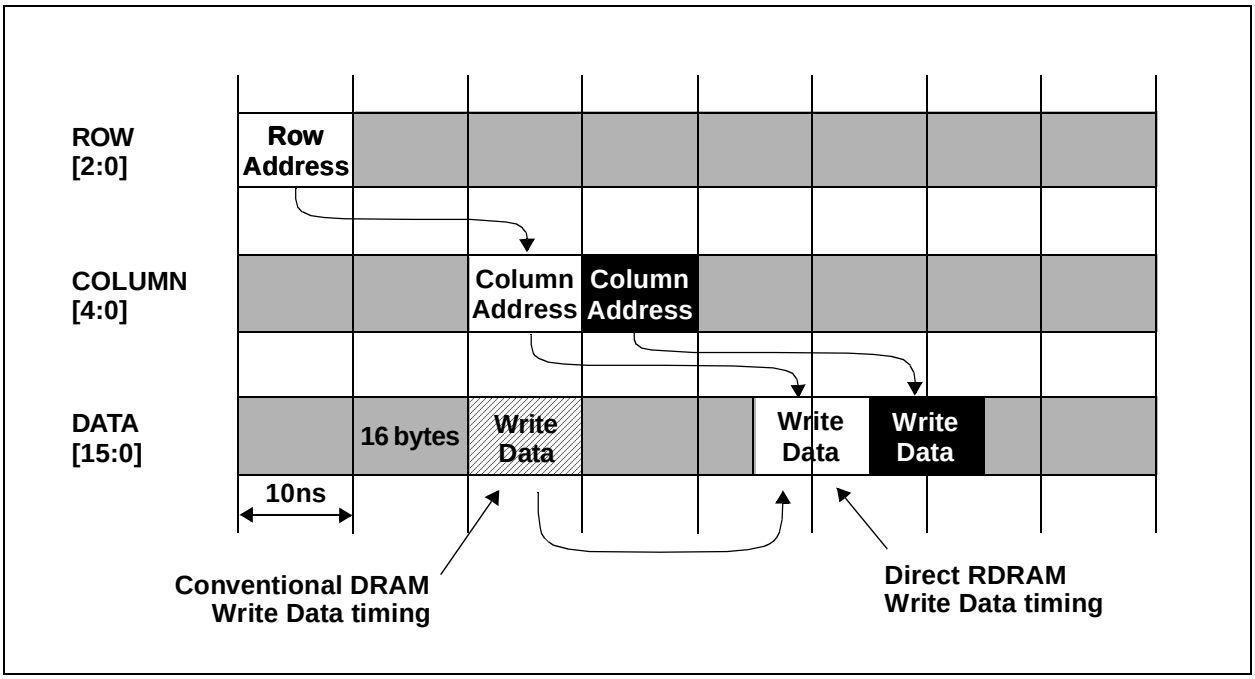

Figure-2 Write Transaction

Careful consideration of high-speed transmission line effects allows the Rambus Channel to achieve its high bandwidth data exchange. The Rambus Channel consists of a set of terminated transmission lines. The RDRAMs are designed to properly drive this terminated transmission line. The RDRAM package is designed to reduce "lead" inductance, allowing the RDRAMs to drive and receive the high frequency bus signals. Bus line length is also reduced. Delay locked loops (DLLs) are used to compensate for the delays of the I/O circuits, allowing the RDRAM to sample its inputs and drive its outputs at precisely the correct time, which is essential when data is valid for less than 1.25 ns. The memory core in the RDRAM is a slightly modified version of the conventional memory array. The modifications are necessary to increase the internal bandwidth to the memory core by increasing the number of bits that are read or written on each cycle.

To test the Direct RDRAM device, the test system must provide differential clock signals of at least 400 MHz and a drive and compare of at least 800 MHz DNRZ data rates to each I/O pin. The HP 95000 HSM Series test system delivers 500 MHz clocks (RZ) and can drive and compare at 1 GHz (DNRZ), thus providing desirable "headroom".

Bus Contention

The next critical issue that needs to be addressed is zero nanosecond bus turnaround time (i.e., no round trip delay) on the bi-directional data pins. Rambus RDRAM devices and most other memory devices in computer systems are bus oriented. Bus contention is a conflict between driving data and receiving data on a common transmission path. It occurs on bi-directional bus lines where the transmission direction can switch according to the I/O cycle being processed. Bus

contention can result in large transient current spikes and may prevent testing at full device speed. Bus contention at the DUT (in and out data delays from DUT to tester) causes a conflict at the tester end. See Figure-3. This creates a "dead zone" (zone of contention) in which the tester only sees its own driver signal, and not the device output signal. The width of this dead zone is given by $2*T_{pd}$.

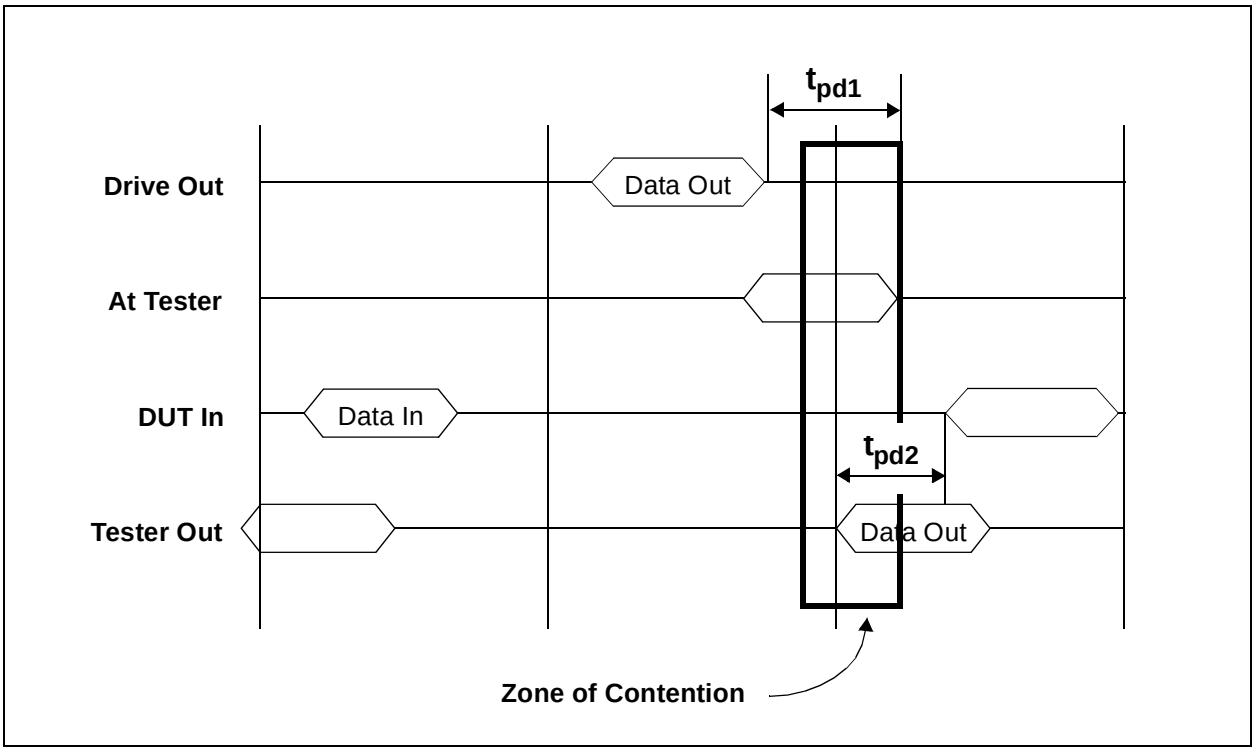

Figure-3 Bus Contention

Creating a round trip delay-free environment allows the DUT and the tester to attain maximum quality high-speed signals and eliminate bus contention errors. Since 1986, when HP introduced the HP 82000, minimizing bus contention has been a design criterion. All high-speed ATE systems today, including the HP 95000 HSM Series test system, use coaxial transmission lines to deliver bi-directional channels to the DUT.

The bi-directional data rate where bus contention occurs is a function of the combined round trip delay of the transmission line of the interface and the loadboard. Bus contention can be solved if the test system supports either a Dual Transmission Line (DTL) or Split I/O arrangement. With the tester channel in either one of these two arrangements, the signals propagate to the end of the transmission lines without any reflections.

Consider the DTL type tester channel arrangement, used by the HP 82000 and HP 83000 test systems and shown in Figure-4. The tester's receiver channel only senses data that propagates

around the clockwise loop. The impedance seen by the DUT consists of two 50 Ohm parallel transmission lines terminated at the end of the each line with matching impedance. This permits the test system to drive I/O lines instantaneously with zero turnaround time.

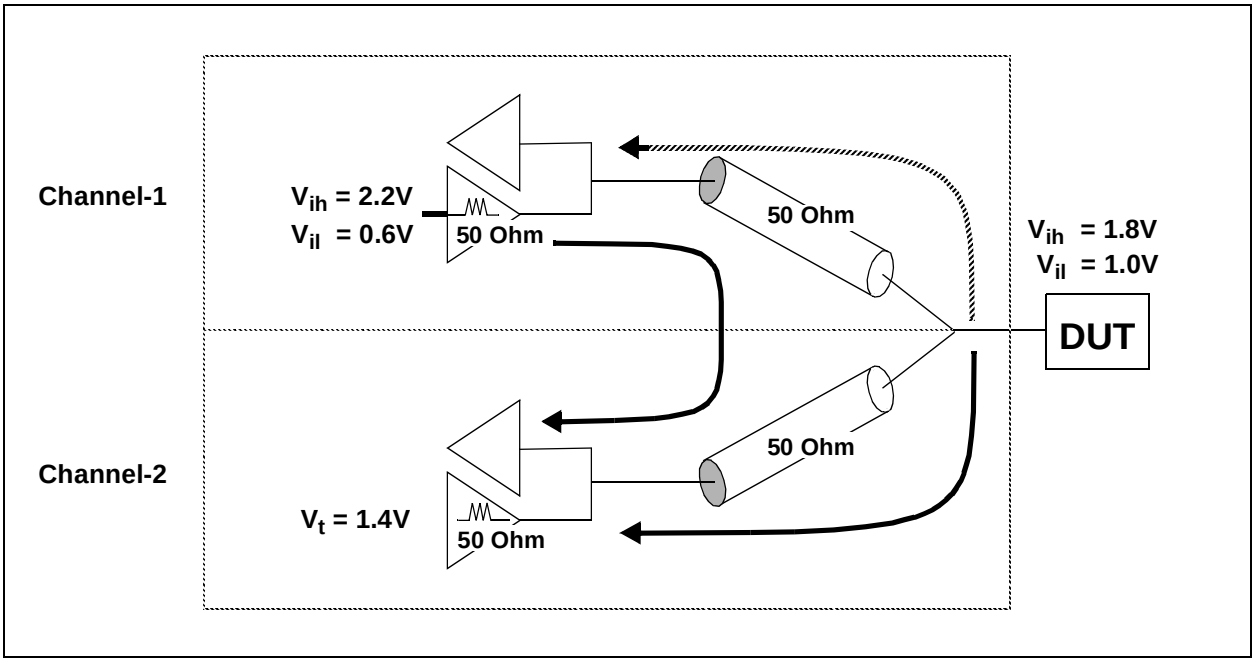

Figure-4 DTL Arrangement for Direct RDRAM

In this case, the data rate is only limited by the tester's minimum drive pulse width and the DUT itself. However, because of the 25 Ohm impedance seen by the DUT, correct V_{il}/V_{ih} values must be recalculated. Direct RDRAM signaling levels are V_{il}=1.0V and V=1.8V_{ih} and the reference voltage level is set to 1.4V, with the termination voltage set to 1.4V, so that drive current requirements are symmetrical. At the tester side, the recalculation results in V_{il}/V_{ih} of 0.6V/2.2V. The Split I/O tester channel arrangement is supported by the HP 95000 HSM Series. It produces the same result while eliminating half of the circuitry. See Figure-5.

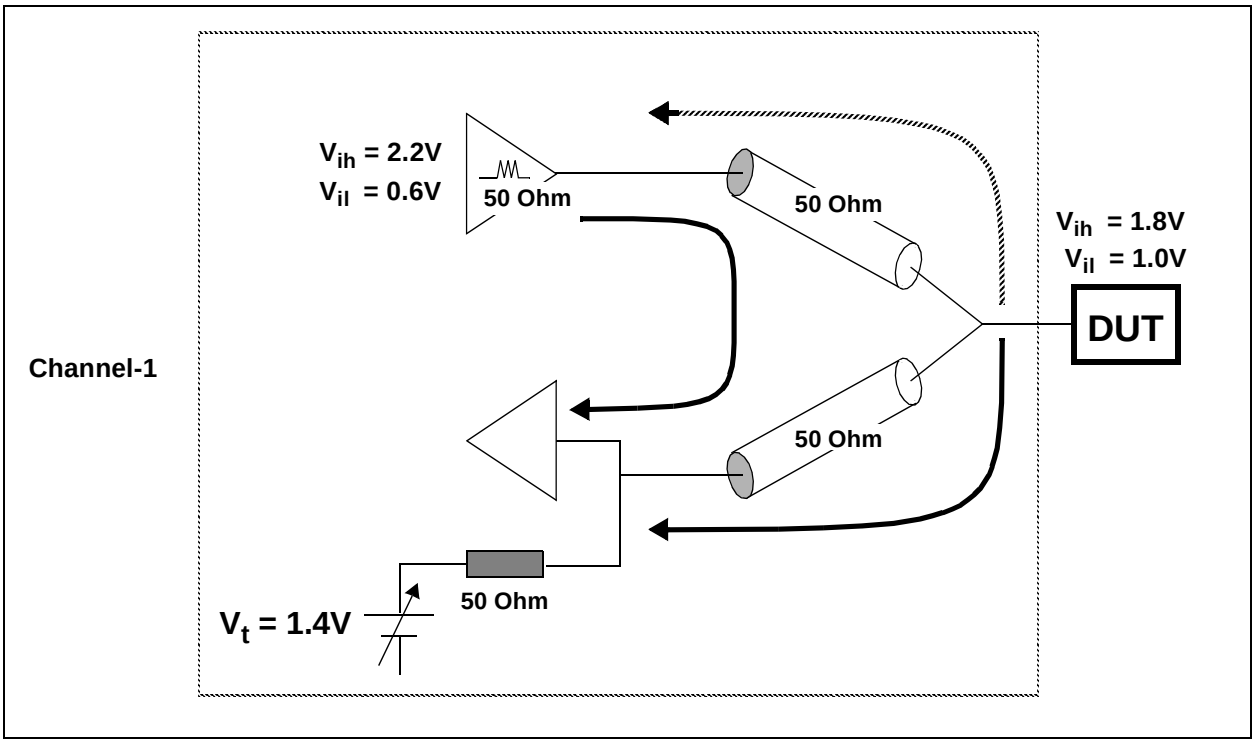

Figure-5 Split I/O Arrangement for Direct RDRAM

DTL or Split I/O solves the bus contention problem at the tester side. On the device side, the Rambus Channel avoids bus contention by using current-mode signaling and by providing non-conflicting signal paths between the Rambus ASIC Cell (RAC) and Direct DRAMs during read/ write cycles, as illustrated in Figure-6.

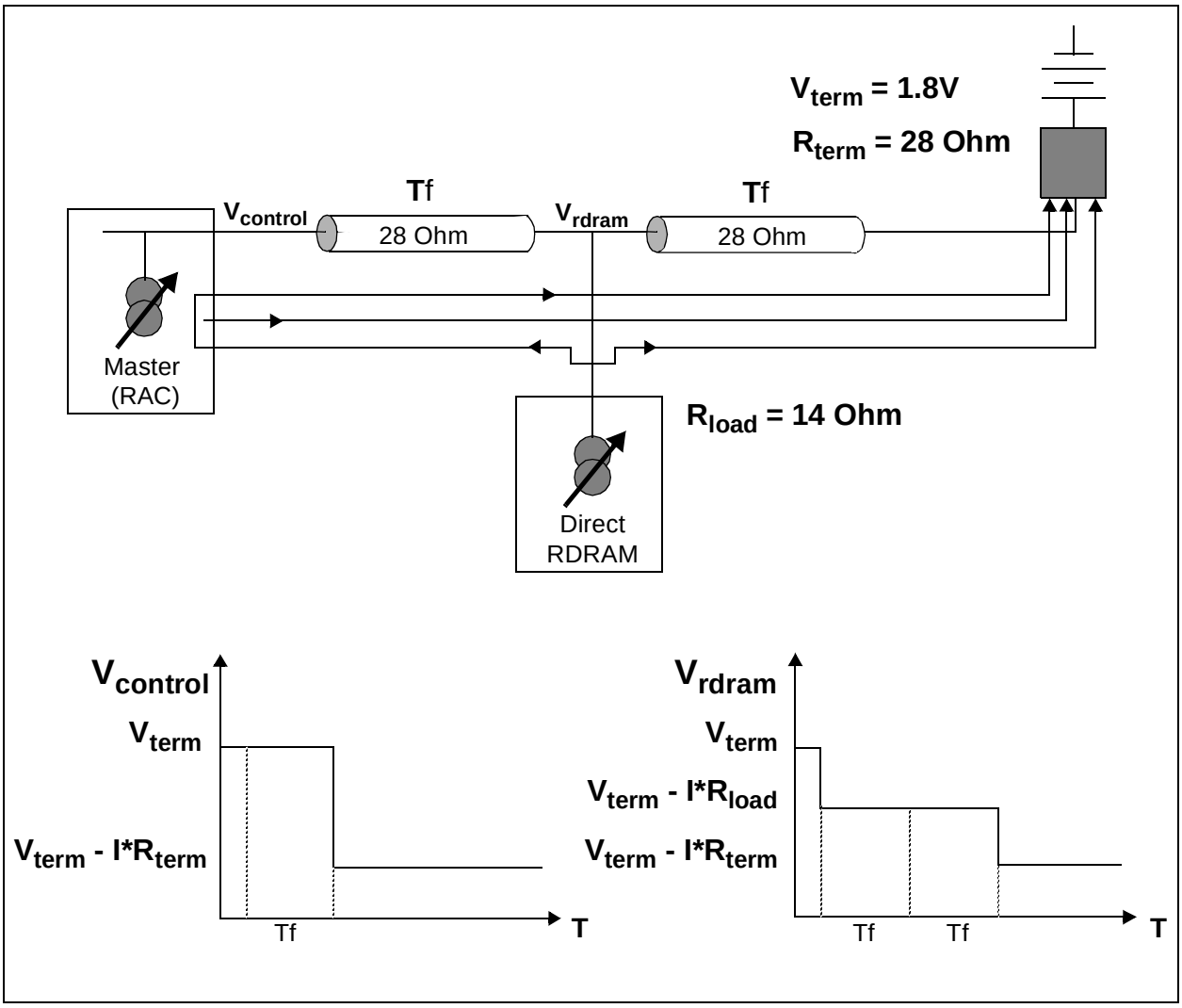

Figure-6 Direct RDRAM Read/Write Operation (RAC Write to BUS, DRDRAM Write to BUS)

A "logic 0" is represented by the termination voltage of 1.8V and "logic 1" is represented by pulling a calibrated current out of the bus. When the memory controller (RAC) wants to drive a logic 1, it sinks enough current to pull the bus down to V_{term} - I*R_{term} and it is terminated at the RDRAM. No further reflection occurs.

The RDRAM device drives a fixed current which results in a half-voltage waveform propagating in both directions (because it is a current mode output) and when the half-voltage swing arrives at the master end it reflects and doubles in amplitude, so that the master sees a full-voltage swing.

Accuracy

Accurate testing of the Direct RDRAM is one of the most challenging issues facing the test engineer, even with excellent loadboard design and proper test fixtures. In addition to providing

accurate waveforms and valid data at > 800 MHz (DNRZ), the test equipment must be able to measure the set-up and hold time of the inputs and the timing of the outputs with high timing accuracy. When the "data cell" is only 1.25 ns wide, i.e., the Rambus Channel latches in 16 (or 18) bits of data every 1.25 ns, the edges must be placed precisely relative to the clock. For the Direct RDRAM, the set-up and hold time specification is < 200 ps.

Tester measurement accuracy (TMA) is a critical element to consider. As illustrated in Figure-7, transmit and receive "test margins," assuming no signal delay caused by the loadboard and contactor, could be calculated as "CLK/2 - 2 * TMA - T_{su}" and "CLK/2 - 2 * TMA - T_q", respectively.

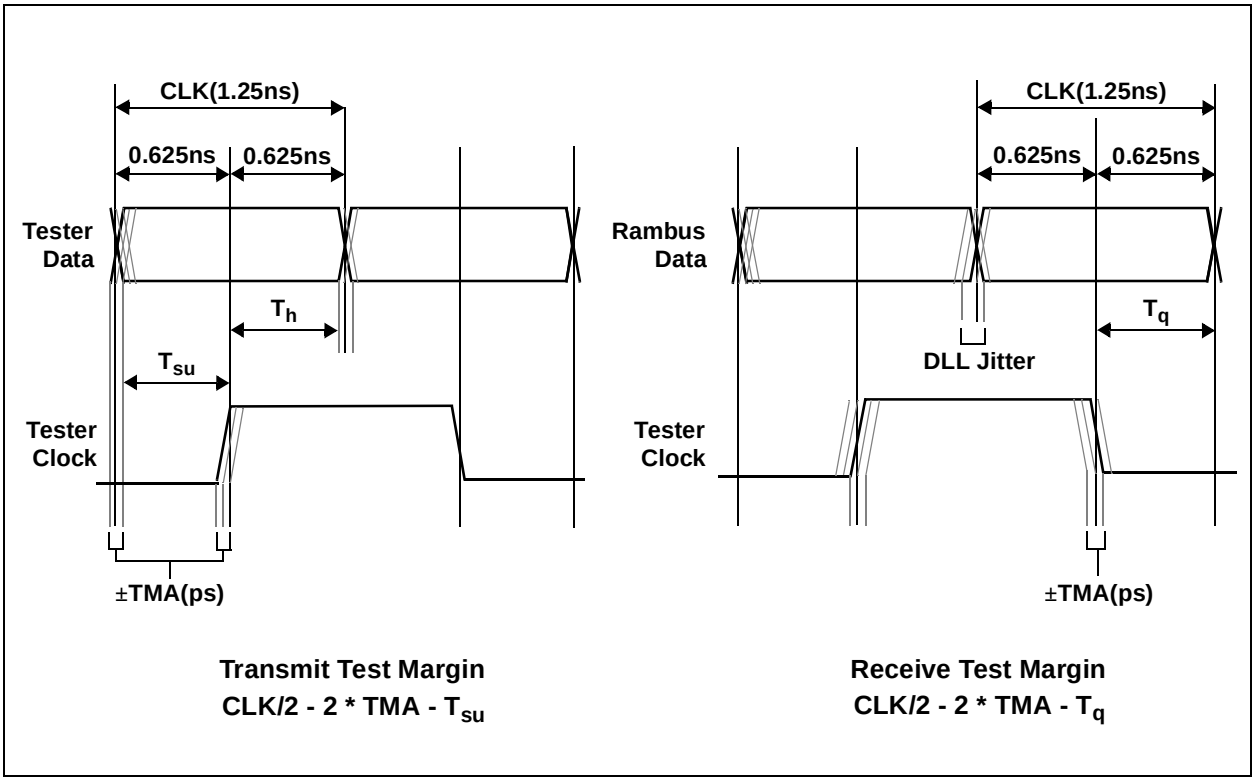

Figure-7 Transmit and Receive Test Margins

A tester with better measurement accuracy allows wider test margins and increased flexibility in testing Direct RDRAM devices. The HP 95000 HSM Series test system utilizes a feature developed with Rambus, called Focused (DUT) Site Calibration, to provide ± 50 ps measurement accuracy for set-up and hold times on RDRAM devices.

Loadboards, DUT Boards, and Contactors

A critical issue pertaining to high speed RDRAM testing is the electrical environment of the DUT. Most of the time it is difficult to create an environment on the tester that closely matches the environment that the device will see in a real system because the production test system environment includes a socket, loadboard, and coaxial cables. Socket inductance, loadboard discontinuities, and coaxial cables degrade the quality of signals to and from the DUT and limit the measured performance of the device. Small parasitic capacitance, discontinuities, or transmission mismatches will quickly use up the test margin. For example, 4pF of lumped capacitance can cause additional signal-edge distortion of 100 ps (R*C/2).

Packaging of the Direct RDRAM device itself is obviously an important consideration, and Table-2 shows the physical interface parameters. With DTL, 52 signal lines are required at the tester since 18 of the 34 DUT signal pins are I/O.

Table 2: Physical Packaging Interface Parameters

Parameter	Direct RDRAM
Package Type	Chip Scale Package (CSP)
Dimensions	12x6.5mm
Ball Pitch	0.75mm
DUT Signal Pins	34

By using a 0.75 CSP, Direct RDRAM can reduce the package size by a factor of four while doubling the number signal lines when compared to Concurrent RDRAM in an SHP type package. Therefore, Direct RDRAM has about eight times more trace lines in a given area than Concurrent RDRAM.

Providing a parallel site loadboard for Direct RDRAM requires designers to carefully consider every aspect of their printed circuit board (PCB) design and be thoroughly familiar with transmission line effects. On a DUT loadboard, the transmission line environment can be disturbed by wiring, vias, soldered-in coax cable, over (or under) etch of the microstrip traces, trace length mismatch, pogo connection, and PCB materials. Use of via holes should be minimized to avoid the loss on transmission lines. If vias are absolutely needed, homogeneous via holes (Z = 50 Ohms) should be created by varying the "via clearance diameter/via hole diameter" ratio. On microstrip corners, a radius or chamfer should be used to avoid abrupt trace angles that cause unwanted reflections at high frequencies. The use of a daughter board for the DUT should be avoided since all signal path discontinuities reduce the accuracy of the measurements.

The above constraints are caused by traditional loadboard pogo configurations where individual DUTs are wired differently. With each additional DUT, wiring becomes exponentially more difficult. The HP 95000 solution (see Figure-8) is an interface architecture where all of the DUTs

can be wired identically. This is done through an interconnect path that allows each pogo block to surround the DUT.

Figure-8 HP 95000 HSM Series Pogo Block and Contactor

Crosstalk is another source of signal integrity loss. Commonly used approaches to minimizing crosstalk are to maintain microstrip spacing with a "space/width" ratio of at least three, termination with characteristic impedance and distribution of signal lines through multiple PCB layers. The use of low dielectric PCB material such as Gore-Ply™ should also be considered. All of these techniques contribute to reducing signal attenuation and distortion at high frequencies.

Selecting the proper contactor in a high-speed testing environment requires special attention because large socket inductance can reduce the quality of the signals dramatically. When locating a contactor, the stub distance should be as small as possible, the contact element should be as small as possible, and the contact area should be as round as possible. Figure-9 illustrates the high performance implementation of the CSP fine-pitch contactor, which is used on the HP 95000 HSM Series high-speed interface. Measurements of the CSP contactor have shown a capacitance of < 1pF, inductance of <1nH, and an insertion loss of 1 dB at 3.5 GHz.

Figure-9 Contactors (16x) and Loadboard Assembly

High accuracy in high frequency testing environments requires a great deal of attention to the DUT board interface and socket interface. However, by eliminating crosstalk and impedance discontinuities, test engineers can produce good signal quality and high signal integrity even with complex devices. By incorporating a high performance interface, loadboard, and contactor, the HP 95000 HSM Series test system is able to provide extremely high accuracy and performance in a high volume production environment.

Conclusion

Preparing to test Direct RDRAMs in high volume production involves two principal choices by the semiconductor manufacturer. One is the selection of the test system(s) to be used, coupled with design concerns for the ancillary hardware necessary to get high quality signals to and from the DUT. Our objective here was to describe those critical issues and to provide some guidance in resolving them.

The other principal choice is that of a test strategy. Guidance in that area is beyond the scope of this paper. It involves factors unique to each semiconductor manufacturer, such as test times for the DRAM core and Rambus interface tests, the relative yields at each of these steps, the availability (and book value) of existing systems for the less demanding tests, throughput requirements, and available space on the test floor.

Since the choices of test system and test strategy are also interrelated in complex ways, suggesting a single overall "best solution" for production testing of Direct RDRAM is an oversimplification. We believe, however, it is possible to determine a "best fit" on a case-by-case basis for individual RDRAM manufacturers when their unique circumstances are considered.

Trademarks

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